Abstract of the Disclosure

A method for controlling a delay time of a signal in a semiconductor device is disclosed, which comprises the steps of: a) applying a test mode pulse signal; b) generating N number of test mode selection signals which are synchronized with the falling edges of the test mode pulse signal to respond sequentially; c) sequentially regenerating the (N-1)th test mode selection signal after the Nth test mode selection signal is generated; and d) repeating step c, wherein an input signal inputted to the semiconductor device is delayed by a predetermined time to be outputted as an output signal only when first to the (N-1)th test mode selection signals are enabled, and the delayed times are different from each other according to the first to the (N-1)th test mode selection signals. In the method, delay degree of a predetermined signal can be freely adjusted in a test mode. Further, a desired delay degree can be set by means of an external signal, regardless of the number of unit delay devices constituting a delay circuit.